2026 Volume: 02 Issue: 04 www.ijrpa.com ISSN 2456-9995 Research Article

International Journal Research Publication Analysis

Page: 01-12

# "PLACEMENT-DRIVEN PHYSICAL IMPLEMENTATION OF A RISC CORE WITH EMBEDDED SRAM USING AN ASIC DESIGN FLOW"

**Dr. Dhilip Kumar P.*[1], Jai Abinav T.[2], Ashwin S.[3], Harini D.[4], Miruthula S.[5]**

[1]Mentor, Department of ECE (VLSI)

[2–5]Undergraduate Students, Department of ECE (VLSI)

**Article Received: 18 March 2026**
**Article Revised: 08 April 2026**
**Published on: 28 April 2026**

***Corresponding Author: Dr. Dhilip Kumar P.**
Mentor, Department of ECE (VLSI), Sri Shakthi Institute of Engineering and Technology, Coimbatore, Tamil Nadu, India.

DOI: https://doi-doi.org/101555/ijrpa.1824

## ABSTRACT

This paper presents a placement-driven physical implementation and optimization of a Reduced Instruction Set Computing (RISC) core integrated with embedded SRAM using a complete ASIC design flow. The design is described at the Register Transfer Level (RTL) using Verilog HDL and functionally verified through FSDB waveform analysis using Verdi. The verified design is synthesized using Synopsys Design Compiler and physically implemented using Synopsys IC Compiler II.

A placement-driven methodology is adopted to improve timing closure, reduce congestion, and optimize area utilization. Experimental results demonstrate a total area of **422.73 µm²**, total power consumption of **24.56 µW**, and a positive slack of **7.60 ns**, indicating successful timing closure. The results highlight that placement-aware optimization significantly enhances design performance and reliability, making the approach suitable for modern low-power VLSI systems.

### Key Contributions of this Work

This work makes the following contributions:

1. Implementation of a complete RTL-to-GDSII flow for a RISC core with embedded SRAM using a placement-driven methodology.
2. Analysis of timing, power, and area trade-offs in a real ASIC design environment.
3. Demonstration of how placement optimization influences congestion, routing efficiency, and timing closure.
4. Identification of clock network dominance in power consumption and its impact on

overall system efficiency.

5. Presentation of a structured design methodology suitable for scalable VLSI systems.

## INDEX TERMS

RISC, ASIC Design Flow, Placement Optimization, Embedded SRAM, Physical Design, VLSI.

## I. INTRODUCTION

The rapid advancement of semiconductor technology has increased the demand for efficient and high-performance integrated circuit design. Reduced Instruction Set Computing (RISC) architectures are widely used due to their simplicity, faster execution, and energy efficiency. The integration of embedded SRAM enhances system performance by enabling faster on-chip memory access.

Physical design plays a crucial role in determining circuit performance, power consumption, and area. Among various stages, placement significantly impacts interconnect delay, congestion, and timing. A placement-driven design methodology ensures optimal positioning of standard cells and macros before routing, leading to improved design quality.

This work focuses on implementing a RISC core with embedded SRAM using a placement-driven ASIC design flow and analyzing its effectiveness in achieving timing closure and congestion reduction.

## II. Background Study

Reduced Instruction Set Computing (RISC) architecture is widely used in modern digital systems due to its simplified instruction set, which enables efficient pipelining and faster execution compared to complex instruction architectures. The reduced complexity of instructions allows better performance, lower power consumption, and improved design scalability.

The ASIC design flow plays a crucial role in transforming a high-level hardware description into a manufacturable integrated circuit. It typically includes stages such as RTL design, functional verification, synthesis, floorplanning, placement, clock tree synthesis (CTS), routing, and physical verification. Each stage contributes to ensuring that the design meets performance, power, and area requirements.

Among these stages, placement optimization is a key factor influencing overall design quality. Placement determines the positioning of standard cells, directly impacting interconnect length, timing path delays, and congestion distribution. An optimized placement reduces wirelength, improves timing closure, and enhances routability, thereby minimizing design iterations in later stages.

The integration of embedded SRAM introduces additional challenges in physical design. SRAM macros impose strict placement constraints, often creating routing blockages and congestion in nearby regions. Furthermore, the presence of memory blocks affects timing due to increased interconnect complexity and limited routing resources around macro boundaries. Addressing these challenges is essential for achieving an efficient and reliable design.

## III. Aim and Objectives

The primary aim of this work is to implement and optimize a RISC core with embedded SRAM using a placement-driven physical design methodology. This involves designing the RISC core using Verilog HDL, performing functional verification through simulation, and generating a gate-level netlist via synthesis. The design is further processed through floorplanning and macro placement, followed by placement-driven optimization to improve timing and reduce congestion. Finally, timing closure is achieved, and the complete physical design is realized through the generation of a GDSII layout suitable for fabrication.

## IV. Design Flow Implementation

The proposed RISC core with embedded SRAM is implemented using a complete RTL-to-GDSII ASIC design flow, ensuring a structured transition from high-level design to physical layout. The design process begins with RTL modeling and progresses through synthesis, placement, and routing, ultimately producing a manufacturable layout.

### A. RTL Design and Functional Verification

The RISC core is designed using Verilog HDL at the Register Transfer Level (RTL), ensuring modularity and scalability of the architecture. A comprehensive testbench is developed to validate the functional correctness of the design under various input conditions. Simulation is performed, and waveforms are generated in FSDB format and analyzed using Verdi. The waveform analysis confirms correct signal transitions, synchronization of control and data paths, and proper operation of sequential elements. Functional verification at this stage ensures that the design is free from logical errors before proceeding to synthesis.

### B. Synthesis

The verified RTL design is synthesized into a gate-level netlist using Synopsys Design Compiler. During this stage, the design is mapped to a standard cell library, and timing constraints are applied to meet performance requirements. The synthesis process involves:

- Conversion of RTL description into an optimized gate-level netlist
- Application of timing constraints to guide optimization
- Optimization for area, power, and timing

This stage ensures that the design is structurally optimized and ready for physical implementation.

### C. Physical Design

The synthesized netlist is implemented physically using Synopsys IC Compiler II, which transforms the logical design into a geometric layout suitable for fabrication. The physical design process consists of multiple stages, each contributing to the final performance and reliability of the chip.

#### 1) Floorplanning

In the floorplanning stage, the overall chip layout is defined by specifying the core area, aspect ratio, and placement of macros and IO pins. Special attention is given to SRAM macro placement to minimize routing congestion and improve accessibility. The key tasks include:

- Defining core dimensions and utilization
- Strategic placement of SRAM macros
- IO pin placement to ensure efficient signal flow

A well-planned floorplan lays the foundation for efficient placement and routing.

#### 2) Placement

Placement involves arranging standard cells within the defined core area. A placement-driven optimization approach is used to improve timing and reduce congestion. The process includes:

- Placement of standard cells based on connectivity and timing requirements
- Optimization to minimize wirelength and critical path delays
- Reduction of congestion, especially near SRAM macro regions

This stage plays a crucial role in determining timing performance and routability of the design.

### 3) Clock Tree Synthesis (CTS)

Clock Tree Synthesis is performed to distribute the clock signal uniformly across the design. A balanced clock network is generated to minimize skew and ensure synchronized operation of sequential elements. The CTS stage includes:

- Construction of clock distribution network
- Minimization of clock skew and insertion delay
- Buffer insertion to balance clock paths

Proper clock distribution is essential for reliable timing behavior.

### 4) Routing

Routing establishes the physical connections between all components in the design. Both global and detailed routing are performed while adhering to design rule constraints. The routing stage ensures:

- Complete connectivity of all nets
- Compliance with design rule checks (DRC)
- Efficient utilization of metal layers

Successful routing confirms that the design is physically realizable.

### 5) GDSII Generation

In the final stage, the completed physical layout is exported in GDSII format, which represents the final mask data required for fabrication. This stage signifies that the design has successfully passed through all implementation steps and is ready for manufacturing.

## V. RESULTS AND DISCUSSION

The proposed methodology emphasizes placement-driven optimization as a critical stage in physical design. Unlike conventional flows where placement is treated as an intermediate step, this approach prioritizes placement quality to improve downstream processes such as clock tree synthesis and routing.

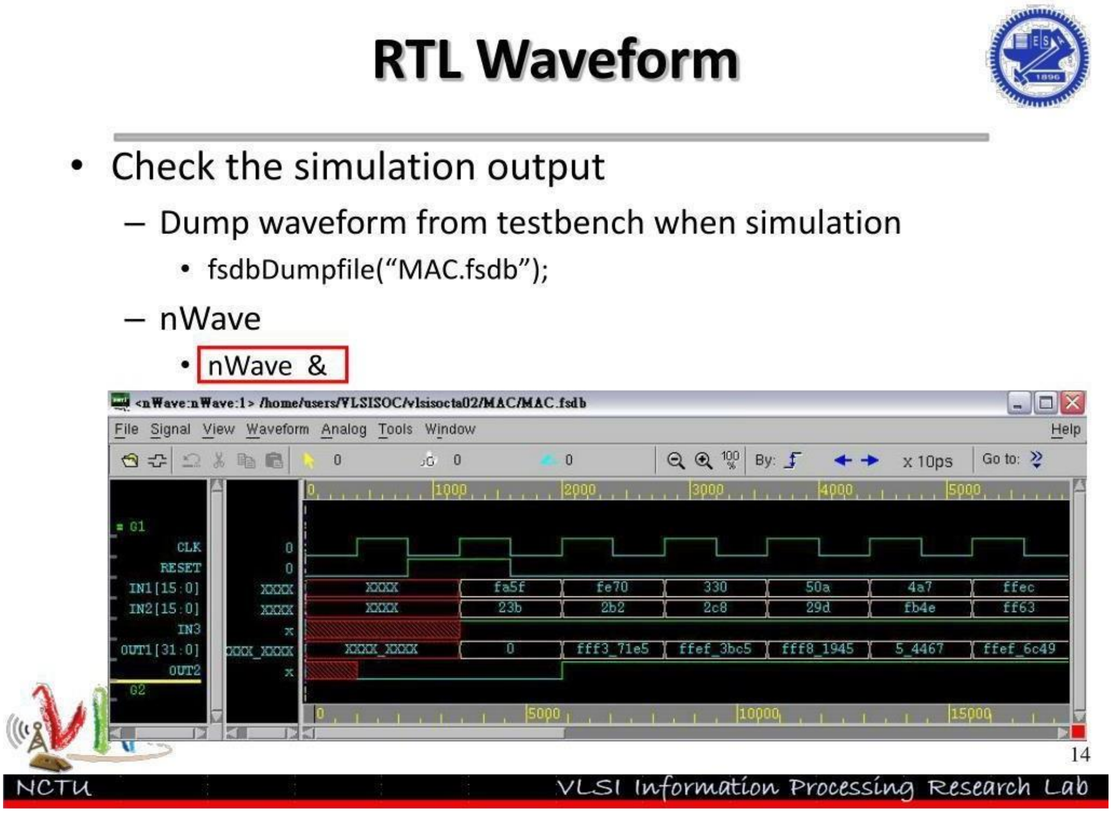
Special attention is given to:

- Minimizing wirelength to improve timing

- Avoiding congestion near critical regions
- Ensuring uniform cell distribution
- Improving routability and signal integrity

This approach results in better timing closure and reduced design iterations.

### 5.1 Functional Verification



RTL Waveform

- Check the simulation output
  - Dump waveform from testbench when simulation
    - fsdbDumpfile("MAC.fsdb");
  - nWave
    - nWave &

14

NCTU VLSI Information Processing Research Lab

The functional verification of the RISC core was carried out using FSDB waveform analysis in Verdi. The simulation results confirm correct operation of key signals including clock, reset, address, and data paths.

- Stable clock transitions observed
- Correct sequential address increment
- No functional mismatches detected
- Proper synchronization between control and data signals

This verifies that the RTL design is functionally correct before synthesis.

### 5.2 Synthesis Results

The RTL design was synthesized using Synopsys Design Compiler with SAED32nm technology library.

**Area Report:**

- Total Cell Area: **356.05 µm²**
- Total Area (including interconnect): **422.73 µm²**
- Combinational Area: **149.18 µm²**
- Sequential Area: **206.87 µm²**

**Timing Report:**

- Worst Negative Slack (WNS): **+7.60 ns (MET)**

**Interpretation:**

The positive slack indicates that the design **meets timing constraints comfortably**, with sufficient margin for reliable operation.

### 5.3 Power Analysis

**Power analysis results:**

- Total Dynamic Power: **18.61 µW**
- Leakage Power: **5.95 µW**
- Total Power: **24.56 µW**

**Power Distribution:**

- Clock Network: **69.21%** (dominant contributor)
- Registers: **20.30%**
- Combinational Logic: **10.49%**

**Interpretation:**

The clock network dominates power consumption, which is typical in synchronous ASIC designs. This suggests potential for optimization using clock gating techniques.

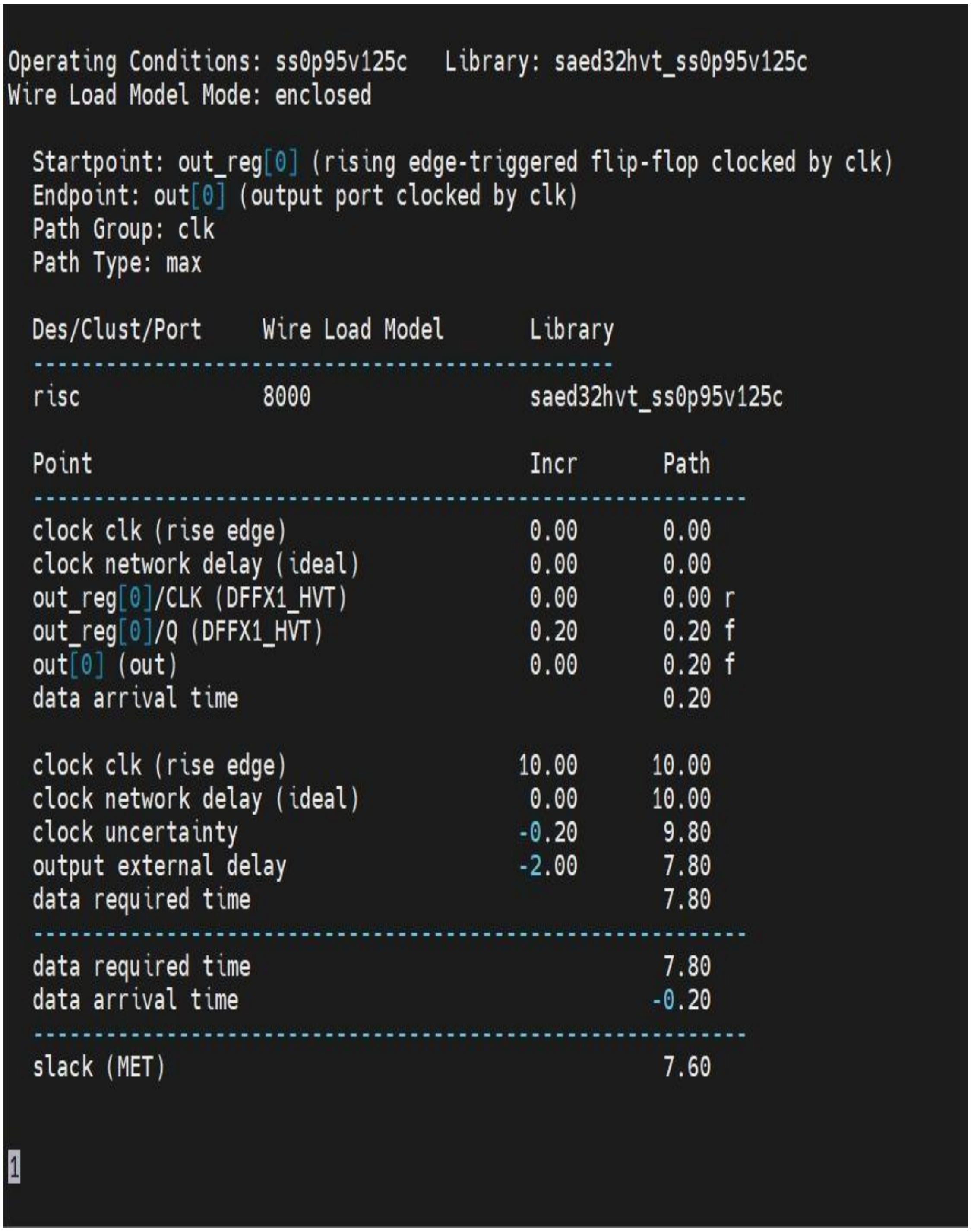
### 5.4 Physical Design Results

The physical implementation was completed using Synopsys IC Compiler II. Observations:

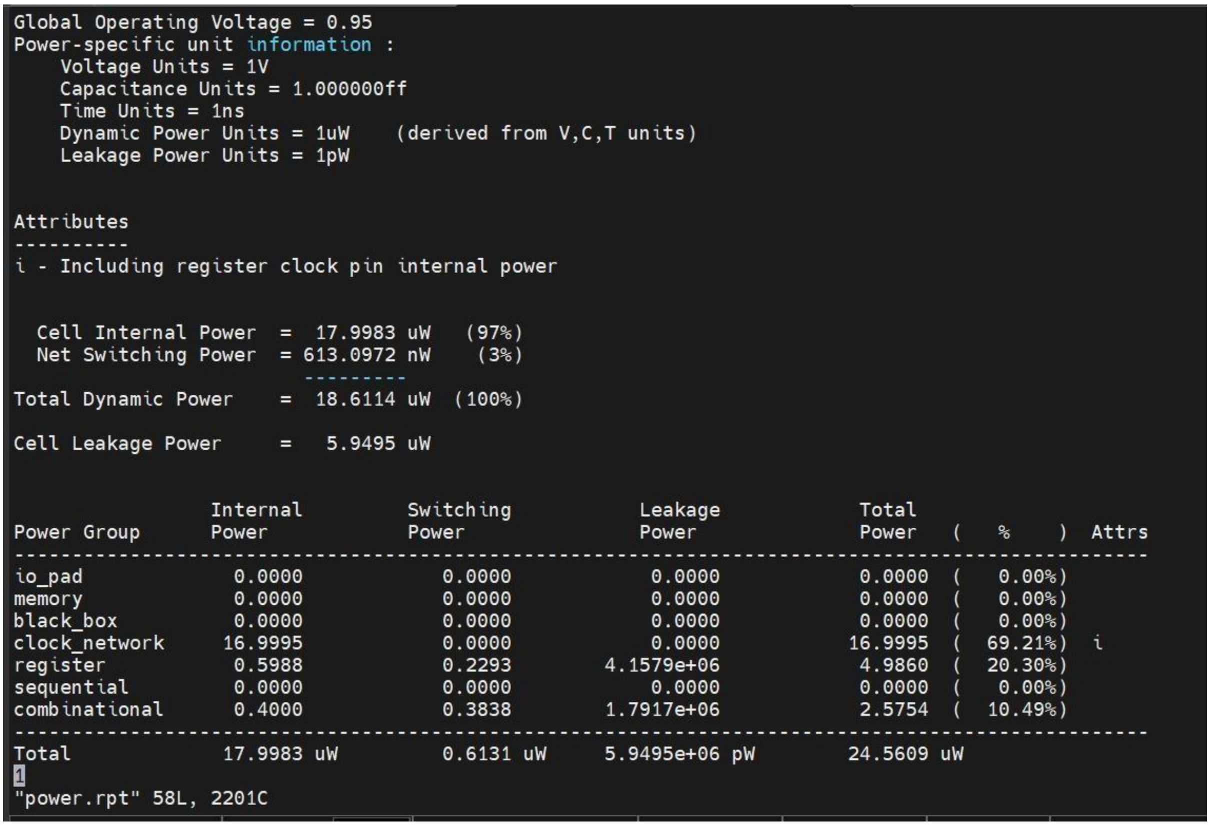
- Successful placement of standard cells

- Uniform cell distribution across core area
- No major congestion hotspots observed
- Routing completed with minimal violations

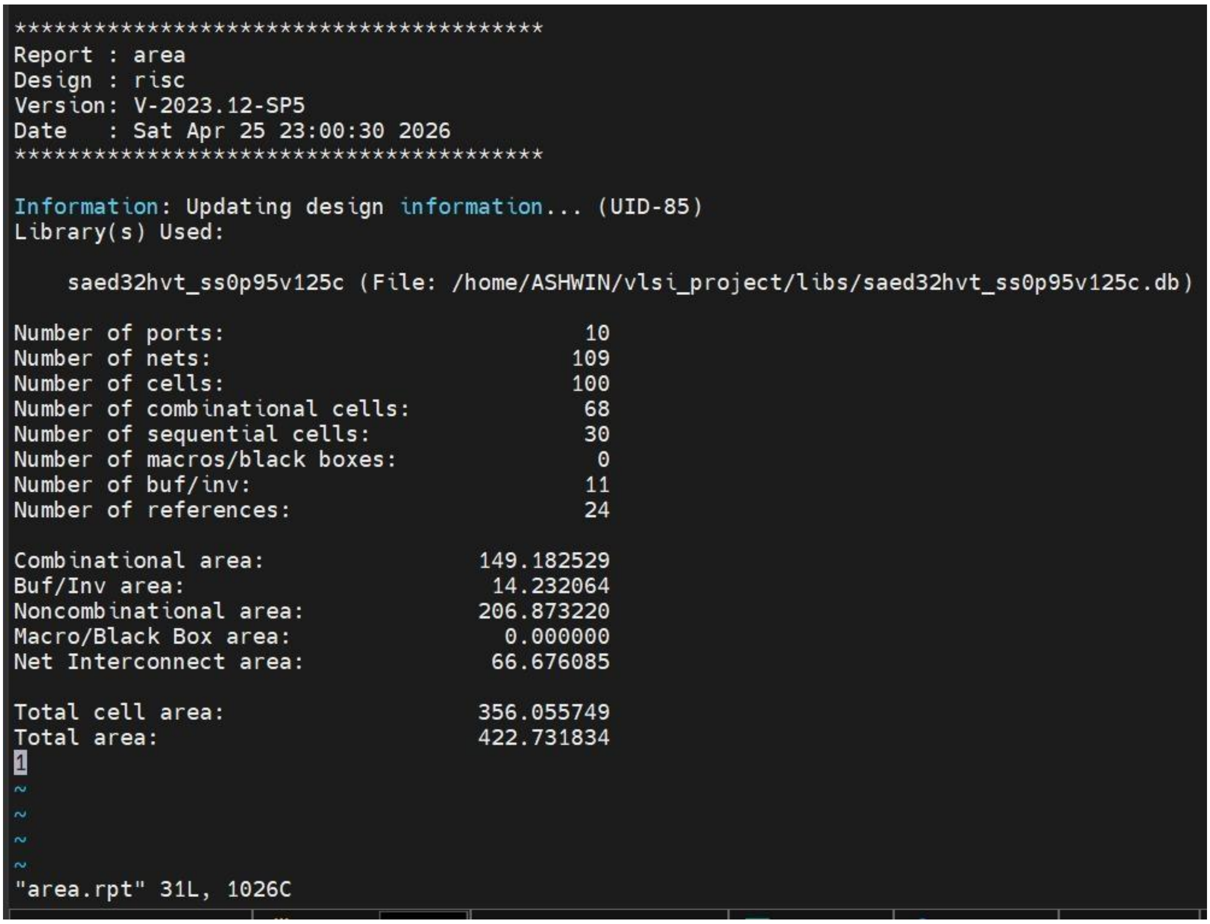
The layout demonstrates efficient utilization of routing layers and proper connectivity across the design.



```
Operating Conditions: ss0p95v125c   Library: saed32hvt_ss0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: out_reg[0] (rising edge-triggered flip-flop clocked by clk)
  Endpoint: out[0] (output port clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  risc               8000                  saed32hvt_ss0p95v125c

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  out_reg[0]/CLK (DFFX1_HVT)               0.00       0.00 r
  out_reg[0]/Q (DFFX1_HVT)                 0.20       0.20 f
  out[0] (out)                             0.00       0.20 f
  data arrival time                                   0.20

  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  clock uncertainty                       -0.20       9.80
  output external delay                   -2.00       7.80
  data required time                                  7.80
  -----------------------------------------------------------
  data required time                                  7.80
  data arrival time                                  -0.20
  -----------------------------------------------------------
  slack (MET)                                         7.60


1
```



```
Global Operating Voltage = 0.95
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


Attributes
----------
i - Including register clock pin internal power


  Cell Internal Power  =  17.9983 uW   (97%)
  Net Switching Power  = 613.0972 nW    (3%)
                         ---------
Total Dynamic Power    =  18.6114 uW  (100%)

Cell Leakage Power     =   5.9495 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000            0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000            0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000            0.0000            0.0000            0.0000  (   0.00%)
clock_network     16.9995            0.0000            0.0000           16.9995  (  69.21%)  i
register           0.5988            0.2293        4.1579e+06            4.9860  (  20.30%)
sequential         0.0000            0.0000            0.0000            0.0000  (   0.00%)
combinational      0.4000            0.3838        1.7917e+06            2.5754  (  10.49%)
--------------------------------------------------------------------------------------------------
Total             17.9983 uW         0.6131 uW     5.9495e+06 pW        24.5609 uW
1
"power.rpt" 58L, 2201C
```



```
****************************************
Report : area
Design : risc
Version: V-2023.12-SP5
Date   : Sat Apr 25 23:00:30 2026
****************************************

Information: Updating design information... (UID-85)
Library(s) Used:

    saed32hvt_ss0p95v125c (File: /home/ASHWIN/vlsi_project/libs/saed32hvt_ss0p95v125c.db)

Number of ports:                           10
Number of nets:                           109
Number of cells:                          100
Number of combinational cells:             68
Number of sequential cells:                30
Number of macros/black boxes:               0
Number of buf/inv:                         11
Number of references:                      24

Combinational area:                149.182529
Buf/Inv area:                       14.232064
Noncombinational area:             206.873220
Macro/Black Box area:                0.000000
Net Interconnect area:              66.676085

Total cell area:                   356.055749
Total area:                        422.731834
1
~
~
~
~
"area.rpt" 31L, 1026C
```

## 5.5 DISCUSSION

The placement-driven physical design approach significantly improved the overall design quality. The positive slack of **7.60 ns** indicates strong timing closure, suggesting that the design can operate at higher frequencies if required.

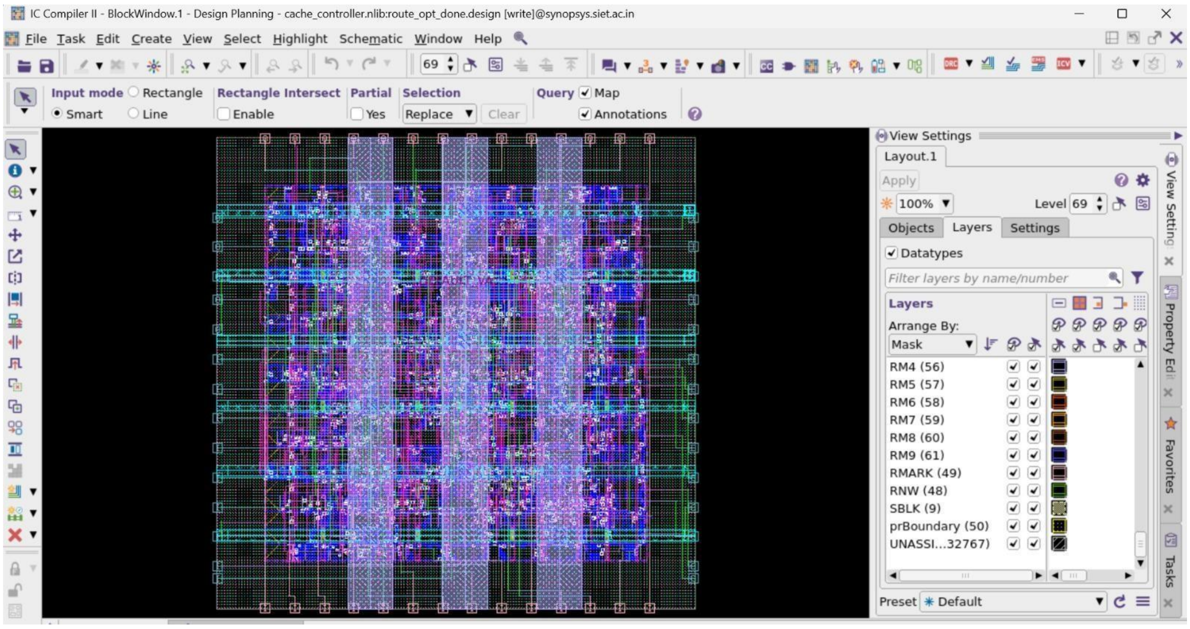
The total area of **422.73 µm²** reflects efficient resource utilization, while the power consumption of **24.56 µW** confirms that the design is suitable for low-power applications.

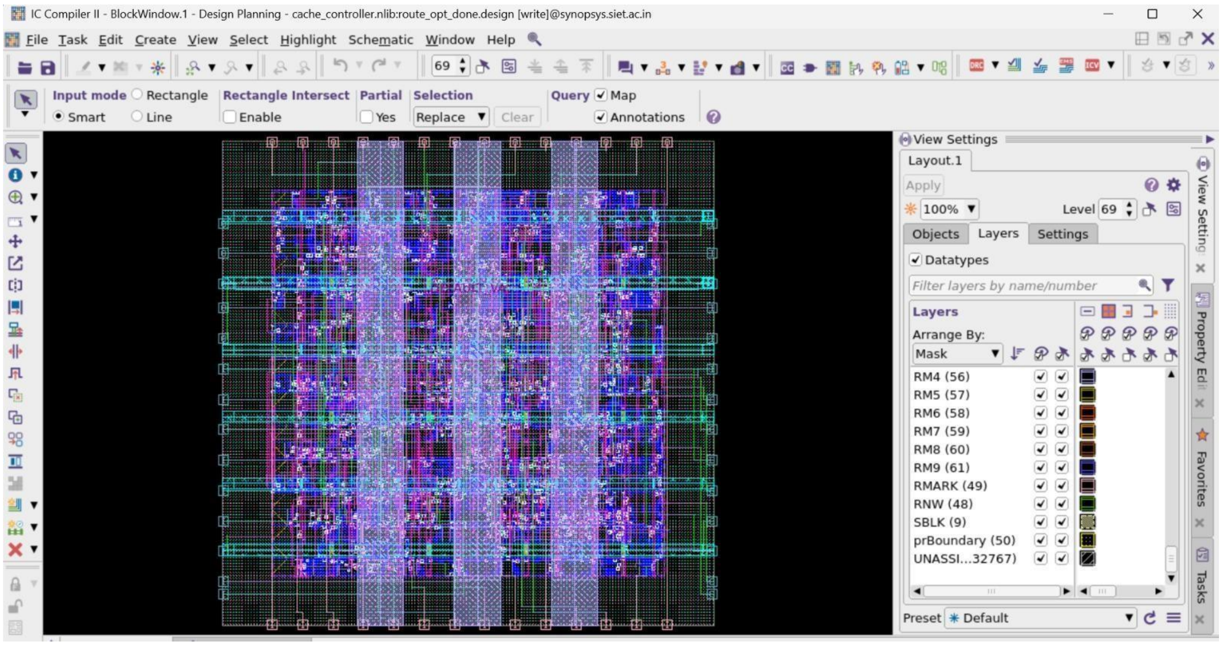
The dominance of clock network power highlights a key optimization opportunity. Future improvements can include:

- Clock gating
- Power-aware placement
- Multi-Vt cell usage

Compared to a conventional flow, the placement-driven methodology provides:

- Better timing performance
- Reduced congestion
- Improved routing efficiency





## CONCLUSION

The placement-driven physical implementation of a RISC core with embedded SRAM has been successfully demonstrated using a complete ASIC design flow. The design achieves a total area of **422.73 µm²**, power consumption of **24.56 µW**, and a positive slack of **7.60 ns**, confirming successful timing closure.

The results clearly indicate that placement plays a crucial role in determining overall design quality. By optimizing placement early in the design flow, improvements in timing, congestion, and routing efficiency are achieved. The observed dominance of clock network power highlights the importance of power-aware optimization techniques in future designs.

This work validates that placement-driven methodologies can significantly enhance ASIC design performance and are well-suited for modern VLSI applications requiring high efficiency and scalability.

## VII. Future work

Future work can focus on:

- Implementation of clock gating techniques to reduce dynamic power
- Power-aware and congestion-driven placement algorithms
- Multi-voltage and multi-threshold (Multi-Vt) optimization
- Integration of larger memory architectures
- Exploration of AI-based physical design optimization techniques

## VII. References

1. N. H. E. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th Edition, Pearson.
   Available: https://www.pearson.com/en-us/subject-catalog/p/cmos-vlsi-design-a-circuits-and-systems-perspective/P200000003256
2. *Synopsys Design Compiler User Guide*.
   Available:https://www.synopsys.com/implementation-and-signoff/rtl-synthesis-test/design-compiler.html
3. *Synopsys IC Compiler II Documentation*.
   Available:https://www.synopsys.com/implementation-and-signoff/physical-implementation/ic-compiler.html
4. IEEE Xplore Digital Library – RISC Architecture Research Papers. Available: https://ieeexplore.ieee.org